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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/750,523
Filing Date: December 31, 2003
Appellant(s): SO ET AL.

Roy B. Rhee
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 7/30/08 appealing from the Office action mailed 10/29/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,500,948	Hinton et al.	3-1996
6,430,670	Bryg et al.	8-2002
6,446,187	Riedlinger et al.	9-2002
Applicant Admitted Prior Art	(AAPA)	

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 12-23, 25, 29-34 and 41-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Hinton et al. (US 5,500,948).

As per **claims 12, 16 and 18**, Hinton discloses a method/system of improving the performance of address translation in a translation lookaside buffer comprising using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd; and consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer;

virtual to physical memory address translation comprising a buffer that uses a single page frame number field for storing odd/even page frame numbers comprising: a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer; a first register for mapping an even page frame number to said single page frame number fields; and a second register for mapping an odd page frame number to said single page frame number field

as [**"Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3) "TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts… Bit 12 selects which of the two entries in the TWB are to be used for this address… Registers (106) marked "0" are for even-numbered**

4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14). ***Hinton also explains "first and second logical registers in said TWB resulting in a first hit signal with respect to said first logical register or a second hit signal with respect to said second logical register… F. gating to a physical address bus a stored value in one of said first or second physical address registers associated with said selected hit signal… issuing a machine bus fetch, upon a condition that said upper order bits of said logical address do not equal a stored value in said first or second logical register in said TWB;… M storing in said TWB said logical address and said second physical address upon a condition that said lower order bits are identical" (Col. 7, line 54-Col. 8; line 45).*** **Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer). Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field".**

For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame

number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Appellant].

As per **claims 13, 22, 30, 33 and 42**, Hinton discloses The method of claim 12 wherein said bit corresponds to the least significant bit of said virtual page number **[Hinton discloses this limitation as "A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address" (Column 6, lines 37-63; Figure 3). Appellant's Specification defines a least significant bit as "a least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described)" (Page 3, Paragraph 0026) and Hinton discloses "a logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page… bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB" (Col. 6, lines 38-43) which clearly corresponds to bit 12 (which is defined as the least significant bit of a virtual page number) of a 32-bit logical address, as defined by Appellant]**. Furthermore; it is the Examiner's position that to one of ordinary skill in the art, the position of the "bit obtained from a virtual page number for the purposes of writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer is a matter of design choice as it appears that the invention would perform equally well with (the least significant bit or any other bit within a virtual page number selected to serve the same purpose as disclosed by Hinton and claimed by Appellant)**]**.

As per **claims 14, 20 and 23**, Hinton discloses The method of claim 12 wherein said address translation of said translation look aside buffer is performed by way of using control processor instruction set **[Hinton discloses instructions are "fetched from memory, instruction queues, (52) for temporary instruction storage between memory and the cache, instruction pre-decode (54) and post-decode logic (58), address translation logic (62), cache tag logic (60), and the necessary IFU control logic" (Column 3, lines 57-62) and explains that wherein memory may be external (Column 3, line 49); therefore, using a control processor instruction set]**.

As per **claims 15, 17 and 19**, Hinton discloses The method of claim 12 wherein said consolidating even and odd page frame numbers into said single page frame number fields implements a translation lookaside buffer of reduced size **[With respect to this limitation, Hinton discloses "Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5). Appellant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 – 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size, as claimed (See Figures 3 and 7 and related text)]**.

As per **claim 21**, Hinton discloses A method of implementing a reduced size translation lookaside buffet comprising:

obtaining a bit obtained from a virtual page number of a virtual address;

using said bit to determine which one of two storage registers will be used for:

a) writing page frame number data from said one of two registers into an indexed entry of a single page frame number field of said translation lookaside buffer, said two storage registers comprising a first storage register used for writing even page frame numbers into said single page frame number field when said bit is a first value and a second storage register used for writing odd page frame numbers into said single page frame number field when said bit is a second value, **or** b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is a second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field **[Hinton discloses "the instruction pointer is comprised of logical address bits" (Col. 2, lines 9-10) which corresponds to Appellant's claimed page number wherein "a logical address (81) is separated into three parts… Bit 12 selects which of the two entries in the TWB are to be used for this address… Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the**

logical and physical addresses" (Column 7, lines 5-14) and Figure 3 and explains "the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25) (*which comprises reading from the TWB; which corresponds to Appellant's claimed TLB*) wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text) [wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text) (*which comprises writing into the TWB; which corresponds to Appellant's claimed TLB*) wherein "registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Col. 6, lines 56-59)].

["the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25) (*which comprises reading/retrieving from the TWB; which corresponds to Appellant's claimed TLB*) wherein "registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Col. 6, lines 56-59)] (*which comprises writing into the TWB; which corresponds to Appellant's claimed TLB*)].

Hinton also explains "first and second logical registers in said TWB resulting in a first hit signal with respect to said first logical register or a second hit signal with respect to said second logical register… F. gating to a physical address bus a stored value in one of said first or second physical address registers associated with said selected hit signal (**which comprises reading from on of the registers of TWB, as claimed*****)… issuing a machine bus fetch, upon a condition that said upper order bits of said logical address do not equal a stored value in said first or second logical register in said TWB;… M storing in said TWB said logical address and said second physical address upon a condition that said lower order bits are identical*** **(which comprises writing into one of the registers TWB, as claimed)*** *" (Col. 7, line 54-Col. 8; line 45).*

Hinton discloses **["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) which is of mini/reduced size. Appellant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 – 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size or mini-TLB, as claimed (See Figures 3 and 7 and related text)]**.

For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages),

which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Appellant].

As per **claims 25 and 43**, Hinton discloses The method of Claim 21 wherein said virtual address comprises 32 bits **[Hinton discloses this limitation as "A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB" (Column 6, lines 38-43)]**.

As per **claim 29**, Hinton discloses A method of performing a write operation using a translation lookaside buffer comprising:
using a bit of a virtual page number, said virtual page number stored in a data register; assessing whether a value of said bit of a virtual page number is 0 or 1; translating a first page frame number stored in a first register to a page frame number field of an indexed entry of said translation lookaside buffer if said value is 0; and writing a second page frame number stored in a second register to said page frame number field of said indexed entry of said translation

lookaside buffer if said value is 1, **[Hinton discloses "the instruction pointer is comprised of logical address bits" (Col. 2, lines 9-10) which corresponds to Appellant's claimed page number wherein "a logical address (81) is separated into three parts… Bit 12 selects which of the two entries in the TWB are to be used for this address… Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14) and Figure 3 and explains "the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25) (*which comprises reading from the TWB; which corresponds to Appellant's claimed TLB*) wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text) (*which comprises writing into the TWB; which corresponds to Appellant's claimed TLB*)]**

said indexed entry, comprising a single page frame number field used to reduce the size of said translation lookaside buffer **[With respect to this limitation, Hinton discloses "Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5). Appellant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value"**

(Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 – 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size, as claimed (See Figures 3 and 7 and related text)].

As per **claim 31**, Hinton discloses The method of Claim 29 wherein a control processor is used to verify that said first page frame number and said second page frame number are valid as **["bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB. If these bits mismatch, it is considered a TWB miss, and the physical address from the TWB is considered invalid. If the bits match, it is considered a TWB hit, and the physical address bits 12 through 31 stored in the TWB are driven out to the cache on output cache physical address (83) and/or on output physical address (80) to the physical address bus" (Col. 6, lines 37-63)]**.

As per **claim 32** A method of performing a read operation using a translation lookaside buffer comprising:

using a bit of a virtual page number, said virtual page number stored in virtual page number field of said translation lookaside buffer; assessing whether n value of a bit of a virtual page number is 0 or 1; reading a page frame number stored in a page flame number field of an indexed entry of said translation 10okaside buffer, storing said page frame number into a first register if said value

is 0; and storing said page frame number into a second register if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer **[The rationale in the rejection to claim 29 is herein incorporated]**.

As per **claim 34** A method of probing for a particular virtual page number of an entry in a translation lookaside buffer comprising:

using a virtual page number stored in a first register; comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer; generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number; and storing said identifying number into a second register [**"Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3) "TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts… Bit 12 selects which of the two entries in the TWB are to be used for this address… Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load,**

"one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14). Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer). Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field.

For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Appellant] [See figure 7 and related text].

As per claim 41, A reduced size translation lookaside buffer comprising: a virtual page number field used to store a virtual page number; a page frame number field used to store an even or an odd page frame number, said even or said odd page frame number indicated by a bit from said virtual page number **[The rationale in the rejection to claim 21 is herein incorporated]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al. (US 5,500,948).

As per **claims 24**, Hinton discloses "The method of claims 3 and 1" **[See rejection to claims 3 and 1 above]**; however, Hinton does not disclose expressly that wherein said TLB control processor instruction set comprises a MIPS control processor instruction set.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an instruction set which comprises a MIPS (Millions Instructions Per Second) processor instruction set which is a well-known processor type. One of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system component designs.

Claims 26 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al. (US 5,500,948) in view of Bryg et al. (US 6,430,670).

As per **claims 26 and 44**, Hinton discloses The method of claim 25 but does not disclose expressly that "said virtual page number is defined by bits [31:12] of said 32 bit virtual address."

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to **[define a virtual page number by bits [31:12] or any other bit positions of said 32 bit virtual address]**. Appellant has not disclosed that **[defining a virtual page number within specific bit positions of a virtual address]** provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Appellant's invention to perform equally well with **[a virtual page number defined as bits 13-31 as taught by Hinton]** because **[positions of a virtual page number bits vary depending on the page size used in the virtual mapping and are system-specific as taught by Bryg (Column 4, lines 9-20)]**.

Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al. (US 5,500,948) in view of Riedlinger et al. (US 6,446,187).

As per **claims 27-28**, Hinton discloses The method of claim; however, Hinton does not discloses "wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes" or "wherein said page mask size comprises 4 kilobytes."

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to **[use a page mask of any size, including a page mask that ranges from 4 kilobytes to 16 megabytes or that comprises 4 kilobytes for virtual to physical address mapping, such as the system taught by Hinton]**. Appellant has not disclosed that **[having a**

virtual address utilize a page mask ranging from 4 kilobytes to 16 megabytes or a page mask of 4 kilobytes] provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Appellant's invention to perform equally well with **[any size of page mask]** because **[it is well known in art that a page mask is used to select a virtual page size (See Riedlinger, Column 4, lines 14-23)]**.

Claims 35-38 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Hinton et al. (US 5,500,948).

As per **claim 35**, AAPA discloses A translation lookaside buffer system comprising: a translation lookaside buffer; **["TLB 104" (Appellant's Specification; Figure 1 and related text)]**

a first register used for storing a value that indexes an entry in said translation lookaside buffer, said entry comprising a virtual page number field and a single page frame number field; **["index 132" (Appellant's Specification; Figure 1 and related text)]**

a second register used for storing a page size of said entry; **["page mask 136" (Appellant's Specification; Figure 1 and related text)]**

a third register used for storing a virtual page number of said entry, said virtual page number comprising a bit; **["Entry Hi" (Appellant's Specification; Figure 1 and related text)]**

a fourth register used for storing an even page frame number; **["entry Lo0" (Appellant's Specification; Figure 1 and related text)]**

and a fifth register used for storing an odd page frame number, **["entry Lo1" (Appellant's Specification; Figure 1 and related text)]**.

AAPA does not disclose expressly said bit of said virtual page number used to determine whether said even page frame number or said odd page flame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page flame number is to be stored in said fourth register or ~aid odd page frame number is' to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer.

Hinton discloses said bit of said virtual page number used to determine whether said even page frame number or said odd page flame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page flame number is to be stored in said fourth register or ~aid odd page frame number is' to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer as **[Hinton discloses "the instruction pointer is comprised of logical address bits" (Col. 2, lines 9-10) which corresponds to Appellant's claimed page number wherein "a logical address (81) is separated into three parts… Bit 12 selects which of the two entries in the TWB are to be used for this address… Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load,**

"one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14) and Figure 3 and explains "the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25) (*which comprises reading from the TWB; which corresponds to Appellant's claimed TLB*) wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text) (*which comprises writing into the TWB; which corresponds to Appellant's claimed TLB*) wherein "Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5). Appellant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 – 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size, as claimed (See Figures 3 and 7 and related text)].

Applicant Admitted Prior Art (AAPA) and Hinton et al. (US 5,500,948) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the TLB system as taught by APPA and further said bit of said virtual page

number used to determine whether said even page frame number or said odd page flame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page flame number is to be stored in said fourth register or said odd page frame number is' to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer as taught by Hinton.

The motivation for doing so would have been because Hinton discloses **["it is an object of the present invention to provide an address translation mechanism that will translate a logical address from a program counter to a physical address to be used to check an on-chip cache for an instruction" (Col. 1, lines 57-60) for efficient address translation]**.

Therefore, it would have been obvious to combine Applicant Admitted Prior Art (AAPA) with Hinton et al. (US 5,500,948) for the benefit of creating a translation lookaside buffer to obtain the invention as specified in claims 35.

As per **claim 36**, the combination of AAPA and Hinton discloses The method of Claim 35 wherein said read and write operations are performed by way of using a translation lookaside buffer (TLB) control processor instruction set **[Hinton discloses instructions are "fetched from memory, instruction queues, (52) for temporary instruction storage between memory and the cache, instruction pre-decode (54) and post-decode logic (58), address translation logic (62), cache tag logic (60), and the necessary IFU control logic" (Column 3, lines 57-62) and**

explains that wherein memory may be external (Column 3, line 49); therefore, using a control processor instruction set].

As per **claim 37**, the combination of AAPA and Hinton discloses The method of claim 35; however, Hinton does not disclose expressly that wherein said TLB control processor instruction set comprises a MIPS control processor instruction set.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an instruction set which comprises a MIPS (Millions Instructions Per Second) processor instruction set which is a well-known processor type. One of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system component designs.

As per **claim 38**, the combination of AAPA and Hinton discloses The method of Claim 35 wherein said virtual page number is defined by a 32 bit virtual address **[Hinton discloses this limitation as "A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB" (Column 6, lines 38-43)]**.

As per **claims 40**, the combination of AAPA and Hinton discloses The method of Claim 38 wherein said bit comprises the least significant bit (lsb) of said virtual page number **[Hinton discloses this limitation as "A logical address (81) is separated into three parts. Bits 0**

through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address" (Column 6, lines 37-63; Figure 3). Appellant's Specification defines a least significant bit as "a least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described)" (Page 3, Paragraph 0026) and Hinton discloses "a logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page… bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB" (Col. 6, lines 38-43) which clearly corresponds to bit 12 (which is defined as the least significant bit of a virtual page number) of a 32-bit logical address, as defined by Appellant]. Furthermore; it is the Examiner's position that to one of ordinary skill in the art, the position of the "bit obtained from a virtual page number for the purposes of writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer is a matter of design choice as it appears that the invention would perform equally well with (the least significant bit or any other bit within a virtual page number selected to serve the same purpose as disclosed by Hinton and claimed by Appellant)].

Claims 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Hinton et al. (US 5,500,948) as applied to claim 38 above, and further in view of Bryg et al. (US 6,430,670).

As per **claims 39**, the combination of AAPA and Hinton discloses The method of claim 38 but does not disclose expressly that "said virtual page number is defined by bits [31:12] of said 32 bit virtual address."

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to **[define a virtual page number by bits [31:12] or any other bit positions of said 32 bit virtual address]**. Appellant has not disclosed that **[defining a virtual page number within specific bit positions of a virtual address]** provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Appellant's invention to perform equally well with **[a virtual page number defined as bits 13-31 as taught by Hinton]** because **[positions of a virtual page number bits vary depending on the page size used in the virtual mapping and are system-specific as taught by Bryg (Column 4, lines 9-20)]**.

(10) Response to Argument

Response to Advisory Action

Appellant has provided arguments in response to Advisory Action mailed on January 8, 2008; however, these arguments parallel arguments presented regarding rejection of claims 12-44 and have been addressed in the same manner. See bellow.

For the most part, Appellant appears to be reading limitations into the claims which are not being claimed; however, the claims have been interpreted according to the broadest

reasonable interpretation available to one of ordinary skill in the art wherein limitations that are not recited in the claims have not been read into the claims (M.P.E.P. 2111 [R-1]).

I. Rejection of Claims 12-23, 25, 29-34 and 41-43 under 35 U.S.C. 102(b) by Hinton

A. Independent claim 12

Appellant argues Hinton does not disclose "consolidating even and odd page frame numbers into a single page frame number field" as recited by claim 12 as Hinton utilizes two separate memories to store even and odd pages, as a consequence, the method disclosed by Hinton provides no reduction in memory size.

In response, this argument has been fully considered, but it is not deemed persuasive.

First, the Examiner would like to respectfully point out that pending claim 12 has been interpreted according to the broadest reasonable interpretation wherein limitations requiring reduction in size or requiring the same or separate memories to define a single field are not recited in the rejected claim 12. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The limitation "a single field" (as claimed) has been interpreted according to the broadest reasonable interpretation wherein a field is known in the art as a location in which a particular type of data is stored (Refer to *Microsoft Computer Dictionary, Fifth Edition*). Note that in Hinton, the combination of registers 104 and 106 is used to store logical and physical address sets (which comprises a particular type of data); therefore, the combination of these registers has

been interpreted as a single field in which logical to physical address sets or a particular data type is stored **[Refer to Hinton (col. 6, lines 37-63; fig. 3 and related text)]**.

The Examiner would also like to point out that Appellant's Specification describes storing even and odd page frame numbers into a single page frame number field of said translation lookaside buffer as **["Figure 3 is a relational block diagram illustrating an organizational structure of a mini- TLB system 300 in accordance with an embodiment of the invention. The mini-TLB system 300 comprises a miniature version of the previously mentioned translation lookaside buffer described in Figure 1 (herein termed a mini-TLB 304) communicating with a number of mini-TLB registers 308 and a control processor 324. In one embodiment, the mini-TLB 304 is configured by way of instructions executed by the control processor 324. For the mini-TLB 304 shown in Figure 3, the index and page mask registers function in the same manner as was described earlier in Figure 1. In addition, virtual addressing is performed using the addressing format described in Figure 2, in which a 32 bit virtual address is used. Of course, it is contemplated that in other embodiments, virtual addressing may be performed using more or less than 32 bits. In the embodiment shown, the entry Hi 312 register of Figure 3 facilitates storage and read out of a virtual page number associated with bits [31:12] of the virtual addressing format discussed previously. Hence, as illustrated in Figure 3, the virtual page number (VPN) may be either read from or written into a VPN field (or section) 316 of the mini-TLB 304. The VPN is associated with a page frame number (PFN) which is similarly either read from or written into a PFN field 320 of the mini-TLB 304 using the registers shown (i.e., entry Lo0 or entry Lol registers). In the embodiment illustrated in Figure 3, only one of the entry Lo**

registers (either entry Lo0 or entry Lol) is valid for use during a write operation; for example, the contents of a valid entry Lo register is written into the page frame number (PFN) field 320 associated with a specified page table entry of the mini-TLB 304. In one embodiment, the least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described) is used to determine whether the entry Lo0 or an entry Lo1 register contains valid data for writing into the PFN field 320 of the mini-TLB 304. Similar principles may be applied during a read from the mini-TLB 304. For example, the least significant bit (lsb) of the VPN may be used to determine which register, either entry Lo0 or entry Lo1, will be used to access valid page frame number data utilized by the control processor 324 during a read operation. In a read operation, for example, the least significant bit (lsb) of a virtual page number is used to store data into either the entry Lo0 register or the entry Lo1 register. In this fashion, both even and odd page frame numbers may be stored or recalled from a single page frame number field of the mini-TLB 304" (Appellant's Specification, Paragraph 0026)]. Therefore, Appellant's Specification discloses two registers and reading/writing to only one of these two registers when reading/writing to TLB. Emphasis added on underlined portions.

In light of the foregoing, Hinton discloses "consolidating even and odd page frame numbers into a single page frame number field" as according to Hinton's disclosure; **[when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into**

a single field within Physical Register 1 (which is used for odd pages), which comprises consolidating even and odd page frame numbers into a single page frame number field]. Note that registers 104 (odd pages) and 106 (even pages) used to store even and odd logical to physical address sets are interpreted as a single page frame number field for even and odd page frame numbers; even page frame number are only stored in register 106 and odd page frame numbers are only stored in register 104. Therefore, Hinton discloses, "consolidating even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Appellant. Refer to the following in Hinton's disclosure [**"Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3) "TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts… Bit 12 selects which of the two entries in the TWB are to be used for this address… Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14)]**.

Further, the Examine would like to emphasize, that contrary to Appellant's assertion, Hinton discloses reducing the size of the TLB, as a reduction in size is a generic property in Hinton's TWB wherein Hinton discloses **["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) which is of mini/reduced size (thus, a size reduction is a generic property of Hinton's TWB or mini-TLB). Appellant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 – 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size or mini-TLB, as claimed (See Figures 3 and 7 and related text)]**.

Appellant remarks that Hinton does not teach a page frame number field as an even or odd logical and physical address set is not a page frame number field.

In response, this remark has been fully considered, but it is not deemed persuasive.

A page frame comprises a physical address to which a page of virtual/logical memory may be mapped (according to *Microsoft Computer Dictionary, Fifth Edition*), wherein virtual/logical to physical address mappings use page frame number to map virtual/logical pages to physical frames; thus, translation sets of virtual/logical and physical addresses inherently comprises page frame numbers. Therefore, contrary to Appellant's remarks, Hinton discloses a

page frame number (as claimed) as **[Refer to logical address (col. 6, lines 37-44) "the instruction pointer is comprised of logical address bits" (Col. 2, lines 9-10) "TWB is loaded with the logical and physical addresses" (col. 7, lines 12-14 and 43-46) wherein "registers (106) marked "0" are for even-numbered pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63; Figure 3)]**.

Appellant argues Hinton's translation write buffer (TWB) does not teach a translation lookaside buffer (TLB) as Hinton's TWB comprises elements that are functionally different from Appellant's claimed invention.

In response, this argument has been fully considered, but it is not deemed persuasive since features referring to the alleged functional differences are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993); wherein the pending claims simply require a translation lookaside buffer, which Hinton clearly discloses as [**"Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5)**]; therefore, TWB comprises a TLB or translation lookaside buffer, as claimed.

Appellant argues the Examiner has failed to provide a logical explanation as to how Hinton may be used to show a teaching of claim 12 and that "for example, the Examiner has

failed to show a teaching of "using a bit obtained from a virtual page number to indicate whether a page number is even or odd."

This argument has been fully considered; however, the Examiner strongly disagrees as Hinton discloses "using a bit obtained from a virtual page number to indicate whether a page number is even or odd" as **["A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address… registers (106) marked "0" are for even-numbered pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63; Figure 3)]**.

B. Dependent Claim 15

Appellant's arguments directed to the rejection of claim 15, for the most part, reiterate the alleged deficiencies Appellant pointed out with respect to independent claim 12. Accordingly, these arguments are addressed at least in the manner that claim 12 has been addressed above.

Claim 15, however, recites the previously argued (and not recited in claim 12) limitation of "consolidating… implements a translation lookaside buffer of reduced size;" wherein Appellant argues Hinton does not disclose this limitation. However, as pointed out above, this argument is not deemed persuasive as a reduction in size is a generic property in Hinton's TWB wherein Hinton discloses **["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) which is of mini/reduced size. Appellant**

should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 – 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size or mini-TLB (as expressly named by Hinton), as claimed (See Figures 3 and 7 and related text)].

C. Independent claim 16

Appellant's arguments directed to the rejection of claim 16, for the most part, reiterate the alleged deficiencies Appellant pointed out with respect to independent claim 12. Accordingly, these arguments are addressed at least in the manner that claim 12 has been addressed above.

Appellant argues Hinton does not disclose "a buffer that uses a single page frame number field for storing odd/even page frame numbers" as required by claim 16; however, the Examiner strongly disagrees as Hinton discloses **[TWB having a single field for storing odd page frame numbers and a single field for storing even page frame numbers (col. 6, lines 37-63; fig. 3 and related text); thus disclosing a single page frame number field for storing odd/even page frame numbers. Further note that registers 104 and 106 in Hinton are interpreted to correspond to a single field]**. See response to **[A. Independent claim 12]** above.

Further, the limitation "a buffer that uses a single page frame number field for storing odd/even page frame numbers" appearing in system claim 16, has been interpreted intended use, and as such the claim does not require the buffer actually perform the listed functionality of storing odd/even page frame numbers, but merely that the function not be expressly precluded. See MPEP 2106 II(C).

D. Dependent Claim 17

Appellant's arguments directed to the rejection of claim 17, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12 and 15. Accordingly, these arguments are addressed at least in the manner that claims 12 and 15 have been addressed above.

E. Independent Claim 18

Appellant's arguments directed to the rejection of claim 18, for the most part, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12 and 15. Accordingly, these arguments are addressed at least in the manner that claims 12 and 15 have been addressed above.

Appellant specifically states "Hinton's physical register 104 is used to store odd numbered pages while Hinton's physical register 106 is used to store even numbered pages. Thus, Hinton does not disclose ""a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer; a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field;" as recited in Claim 18. Instead, Hinton utilizes two separate memory to store even and odd pages;" however, the Examiner would like to respectfully point to Appellant that Appellant's own claim 18 requires a register for odd numbered page frame numbers and a register for even numbered page frame numbers, which comprise two separate memories. Refer to response to **[A. Independent claim 12]** above.

Appellant argues the Examiner has not shown a teaching of "a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field;" however, the Examiner has identified "a first register for mapping an even page frame number to said single page frame number field" as **[Hinton discloses "A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address… registers (106) marked "0" are for even-numbered pages" (col. 6, lines 37-63; fig. 3 and related text)]** and "a second register for mapping an odd page frame number to said single page frame number field" as **["Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63; fig. 3 and related text)]**.

F. Dependent Claim 19

Appellant's arguments directed to the rejection of claim 19, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12 and 15. Accordingly, these arguments are addressed at least in the manner that claims 12 and 15 have been addressed above.

G. Independent Claim 21

Appellant's arguments directed to the rejection of claim 21, for the most part, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12 and 15. Accordingly, these arguments are addressed at least in the manner that claims 12 and 15 have been addressed above.

Appellant argues Hinton does not disclose a "bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into said single page fame number field." In response, this argument has been fully considered, but it is not deemed persuasive since Hinton clearly discloses **[when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises consolidating even and odd page frame numbers into a single page frame number field]**. Note that registers 104 (odd pages) and 106 (even pages) used to store logical to physical address sets are interpreted as a single page frame number field for even and odd page frame numbers; even page frame numbers are only stored in register 106 and odd page frame numbers are only stored in register 104. Further note that a reduction in size is a generic property in Hinton's TWB wherein Hinton discloses **["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) which is of mini/reduced size]**. Refer to Response to **[A. Independent Claim 12 and B. Dependent Claim 15]** above.

H. Independent Claim 29

Appellant's arguments directed to the rejection of claim 29, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12, 15 and 21. Accordingly, these

arguments are addressed at least in the manner that claims 12, 15 and 21 have been addressed above.

I. Independent Claim 32

Appellant's arguments directed to the rejection of claim 32, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12, 15 and 21. Accordingly, these arguments are addressed at least in the manner that claims 12, 15 and 21 have been addressed above.

J. Independent Claim 34

Appellant's arguments directed to the rejection of claim 34, for the most part, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12, 15 and 21. Accordingly, these arguments are addressed at least in the manner that claims 12, 15 and 21 have been addressed above.

Appellant argues the Examiner does not show a teaching of "using a virtual page number stored in a first register", "comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer" and "generating an identifying number associated with an entry of said one or more entries if a virtual page frame number stores a value that is equal to said virtual page number, and storing said identifying number into a second register".

In response, these arguments have been fully considered, but are not deemed persuasive.

Hinton discloses "using a virtual page number stored in a first register" as **["a logical address (81) is separated into three parts… Bit 12 selects which of the two entries in the TWB are to be used for this address… Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63); TLB comprises another register]**; "Comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer" **[Hinton discloses "the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values" wherein a hit or a miss would be detected (col. 7, lines 24-47)]** and "generating an identifying number associated with an entry of said one or more entries if a virtual page frame number stores a value that is equal to said virtual page number, and storing said identifying number into a second register" **[the value stored in the register wherein a hit is detected is gated to physical address bus, wherein bit 12 would be 0 for even entries and 1 for odd entries and sent to cache, which also comprises a register; wherein it is also taught that when logical address bits 0-11 match, the TWB stores the logical address in one of its entries (col. 6, lines 37-63; col. 7, lines 24-47; figs. 3 and 7 and related text)]**.

K. Independent Claim 41

Appellant's arguments directed to the rejection of claim 41, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12, 15 and 21. Accordingly, these

arguments are addressed at least in the manner that claims 12, 15 and 21 have been addressed above.

Appellant argues Hinton does not disclose "a page frame number field used to store an even or an odd page frame number, said even or said odd page frame number indicated by a bit from said virtual page number;" however, Examiner strongly disagrees as Hinton discloses a page frame number field used to store an even **[register 106 (fig. 3 and related text; col. 6, lines 37-63)]** *OR* (*note that only ever OR odd is required by claim 41, which claims limitations in the alternative form*) an odd **[register 104 (fig. 3 and related text; col. 6, lines 37-63)]** page frame number, said even or said odd page frame number indicated by a bit from said virtual page number **[Hinton discloses bit 12, if zero, selects even page frame number (register 106) OR if 1, selects odd page frame number (register 1047) (fig. 3 and related text; col. 6, lines 37-63)]**. Further Refer to Response to **[A. Independent Claim 12, B. Dependent Claim 15 and G. Independent Claim 21]** above.

II. Rejection of Claim 24 under 35 U.S.C. 103(a) as being unpatentable over Hinton

A. Dependent Claim 24

In response to Appellant's remark that the Examiner does not provide proper motivation to modify Hinton to incorporate a MIPS control processor instruction set as "Appellants do not see how selecting from off the shelf processors at least to reduce cost and take advantage of existing component design has anything to do with combining the teachings of Hinton with a MIPS control processor instruction set."

In response, this remark has been fully considered, but it is not deemed persuasive.

Sources of rationale supporting a rejection under 35 U.S.C. 103 may be in a reference, or reasoned from common knowledge in the art, scientific principles, art recognized equivalents, or legal precedent. The CCPA has held that "in considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom."

***In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968); MPEP 2144.01**

In determining obviousness under 35 U.S.C. 103 in view of the Supreme Court decision in KSR International Co. v. Teleflex Inc., the Supreme Court stated that: "If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill".

Still further, the Court states that "the focus when making a determination of obviousness should be on what a person of ordinary skill in the pertinent art would have known at the time of the invention…and this is regardless of whether the source of that knowledge and ability was documentary prior art, general knowledge in the art, or common sense".

The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use an existing processor instruction set, such as MIPS (Millions Instructions Per Second) and make the translation lookaside buffer as taught by Hinton compatible with existing instructions, software, or commands as one of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing components. Thus, the examiner has provided a motivation one of ordinary skill would have had to make an invention compatible with a MIPS (Millions Instructions Per Second) processor instruction set, which is a well-known processor type.

In light of the forgoing, Examiner would like to accentuate that Hinton meets the claimed invention, as required by claim 24.

III. Rejection of claims 27 and 28 under 35 U.S.C. 103(a) as being unpatentable over Hinton in view of Riedlinger

A. Dependent Claim 27

Appellant argues "Appellants respectfully disagree that it would have been obvious for one of ordinary skill in the art to "use a page mask of any size, including a page mask that ranges

from 4 kilobytes to 16 megabytes or that comprises 4 kilobytes for virtual to physical address mapping, such as the system taught by Hinton." Furthermore, Appellants respectfully disagree that it would have been obvious to utilize a page mask size ranging from 4 kilobytes to 16 megabytes, as recited in Claim 27," that the Examiner has not produced a prima facie case, thus "the Appellant is under no obligation to submit evidence of unobviousness", and that "the Examiner has not provided any suggestion or motivation, to support this conclusion."

These arguments have been fully considered, but are not deemed persuasive.

First, the Examiner refutes Appellant's argument that the Examiner has not provided a prima facie, as evidence, refer to Final Office Action mailed on 10/29/2007.

The Examiner deems that it would have been obvious to one of ordinary skill in the art to **[use a page mask of any size, including a page mask that ranges from 4 kilobytes to 16 megabytes or that comprises 4 kilobytes for virtual to physical address mapping]** as the size of a page mask is a matter of design choice as it appears that the invention would perform equally well with any size of page mask. The reference to Riedlinger has been provided as proof that it is well known in the art at time of the invention that the page mask size is used to selected a virtual page size.

Note that the page mask size as used in the various aspects of Appellant's claimed invention provides a preferred embodiment (i.e., a preferred range) in which the claimed invention may be realized; wherein it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Furthermore, the recitations of "wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes" or "wherein said page mask size comprises 4 kilobytes;" is a mere change in size of a virtual page mask size. A change is size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Further, refer to response of **[II. A. Dependent Claim 24]** above wherein it is shown that sources of rationale supporting a rejection under 35 U.S.C. 103 may be in a reference, or reasoned from common knowledge in the art, scientific principles, art recognized equivalents, or legal precedent.

B. Dependent Claim 28

Appellant's arguments directed to the rejection of claim 28, reiterate the alleged deficiencies Appellant pointed out with respect to claim 27. Accordingly, these arguments are addressed at least in the manner that claim 27 has been addressed above.

IV. Rejection of Claims 35-38 and 40 under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Hinton

A. Independent Claim 35

Appellant's arguments directed to the rejection of claim 35, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12, 15 and 21. Accordingly, these arguments are addressed at least in the manner that claims 12, 15 and 21 have been addressed above. Refer to rejection to claim 35 in Grounds of Rejection above.

B. Dependent Claim 37

Appellant's arguments directed to the rejection of claim 37, reiterate the alleged deficiencies Appellant pointed out with respect to claim 24. Accordingly, these arguments are addressed at least in the manner that claim 24 has been addressed above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Yaima Campos

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